CLAIMS

What is claimed is:

1. A method of forming copper features on a semiconductor substrate, comprising:

coating the substrate with a copper seed layer to form a composite;

coating the composite with a resist;

exposing the resist to actinic radiation;

developing the resist to expose a portion of the copper seed layer and form a patterned resist coating; and

plating copper to obtain copper features grown from the copper seed layer.

2. The method of claim 1, further comprising:

stripping the resist after plating the copper;

forming a dielectric coating over the copper features; and

removing a portion of the dielectric coating to expose the copper features.

3. The method of claim 2, wherein the portion of the dielectric coating is removed by mechanical polishing.

4. The method of claim 2, wherein the portion of the dielectric coating is removed by chemical-mechanical polishing.

5. The method of claim 2, further comprising, prior to coating with the dielectric, coating the copper features with a diffusion barrier forming material.

6. The method of claim 2, further comprising, prior to stripping the resist, planarizing the copper features and the patterned resist coating.

7. The method of claim 1, further comprising after developing but prior to plating, trimming the patterned resist coating to increase a line width defined by an opening in the patterned resist coating.

8. The method of claim 7, wherein trimming increases the line width by at least about 25%.

9. A method of forming copper features on a semiconductor substrate, comprising:

coating the semiconductor substrate with a resist;

exposing the resist to actinic radiation;

developing the resist to form a patterned resist coating having openings;

forming a copper seed layer over the patterned resist coating and substrate to form a composite;

removing a portion of the copper seed layer outside of the openings;

plating copper to obtain copper features grown from the copper seed layer within the openings of the patterned resist coating.

10. The method of claim 9, further comprising:

stripping the resist;

coating the copper and the exposed substrate with a dielectric; and

removing a portion of the dielectric to expose the copper.

11. The method of claim 10, further comprising, prior to coating with the dielectric, coating the copper with a diffusion barrier forming material.

12. The method of claim 10, further comprising, prior to stripping the resist, planarizing the copper features and the resist.

13. The method of claim 9, further comprising after developing but prior to plating, trimming the patterned resist coating to increase a line width defined by an opening in the patterned resist coating.

14. The method of claim 13, wherein trimming increases the line width by at least about 25%.

15. A composite, comprising:

a semiconductor substrate;

a copper seed layer over the semiconductor substrate; and

a patterned resist coating over and in contact with the copper seed layer.

16. A composite, comprising:

a semiconductor substrate;

a patterned resist coating, having openings, over the semiconductor substrate; and

copper filling the openings in the patterned resist coating.

17. The composite of claim 23, wherein the copper and the patterned resist coating are planarized.

18. A method of forming copper features on a semiconductor substrate, comprising:

coating the substrate with a copper seed layer to form a composite;

coating the composite with a resist;

exposing the resist to actinic radiation;

developing the resist to form a patterned resist coating having openings; and

coating the resist with a dielectric that fills the openings;

polishing to remove dielectric outside the openings;

stripping the resist to expose a portion of the copper seed layer; and

plating copper to obtain copper features grown from the copper seed layer.

19. The method of claim 18, further comprising planarizing the copper features and the dielectric.

20. The method of claim 18, further comprising trimming the dielectric prior to plating to increase a line width defined by an opening in the patterned resist coating.

21. The method of claim 20, wherein trimming increases the line width by at least about 25%.

22. A method of forming copper features on a semiconductor substrate, comprising:

coating the substrate with a copper seed layer to form a composite;

coating the composite with a resist;

exposing the resist to actinic radiation;

developing the resist to form a patterned resist coating having openings; and

coating the patterned resist with a temporary coating that fills the openings in the patterned resist;

polishing to remove the temporary coating outside the openings in the patterned resist;

stripping the resist to expose a portion of the copper seed layer; and

plating copper to obtain copper features grown from the copper seed layer;

stripping the temporary coating;

coating the copper features with a dielectric; and

polishing to expose the copper features.

23. The method of claim 22, further comprising trimming the temporary coating prior to plating to increase a line width defined by an opening in the temporary coating.

24. The method of claim 20, wherein trimming increases the line width by at least about 25%.

25. The method of claim 22, further comprising, prior to coating with the dielectric, coating the copper features with a diffusion barrier forming material.